CHAPTER 8

Multilevel Inverters

After completing this chapter, students should be able to do the following:

- List the types of multilevel inverters.
- Describe the switching technique for multilevel inverters and their types.
- Describe the principle of operation of multilevel inverters.
- List the main features of multilevel inverters and their types.
- List the advantages and disadvantages of multilevel inverters.
- Describe the control strategy to address capacitor voltage unbalancing.
- List the potential applications of multilevel inverters.

Symbols and Their Meanings

Symbols	Meaning
I_o; I_m	Instantaneous and peak output voltages, respectively
V_a; V_b; V_c	Rms voltages of line a, b, and c, respectively
V_{an}; V_{bn}; V_{cn}	Rms phase voltages of phases a, b, and c, respectively
V_{dc}; E_m	Dc supply voltage and capacitor voltage, respectively
m	Number of levels
V_1; V_2; V_3; V_4; V_5	Voltages of level 1, 2, … 5, respectively
V_D	Diode blocking voltage

8.1 INTRODUCTION

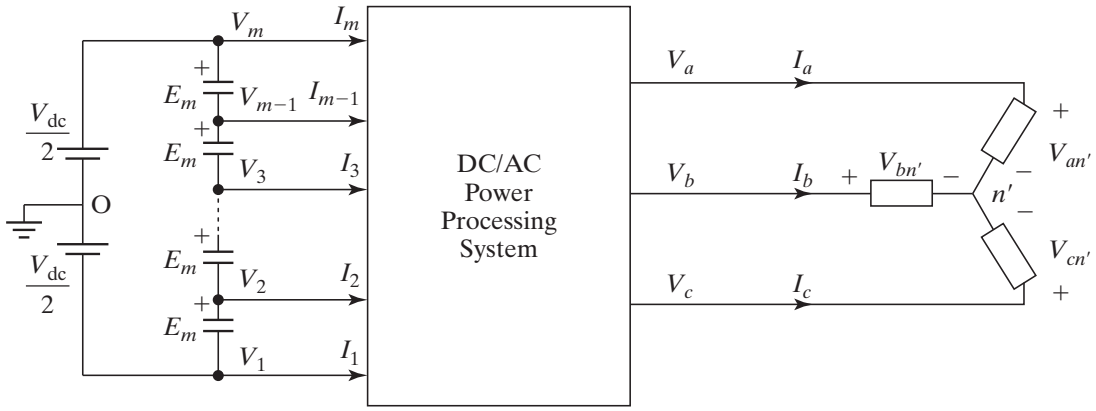
The voltage-source inverters produce an output voltage or a current with levels either 0 or $\pm V_{\text{dc}}$. They are known as the two-level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high-switching frequency along with various pulse-width-modulation (PWM) strategies. In high-power and high-voltage applications, these two-level inverters, however, have some limitations in operating at high frequency, mainly due to switching losses and constraints of device ratings. Moreover, the semiconductor switching devices should be used in such a manner as to avoid problems associated with their series–parallel combinations that are necessary to obtain capability of handling high voltages and currents.

The multilevel inverters have drawn tremendous interest in the power industry, transportation, and renewable energy [12]. They present a new set of features that are well suited for use in reactive power compensation. It may be easier to produce a high-power, high-voltage inverter with the multilevel structure because of the way in which

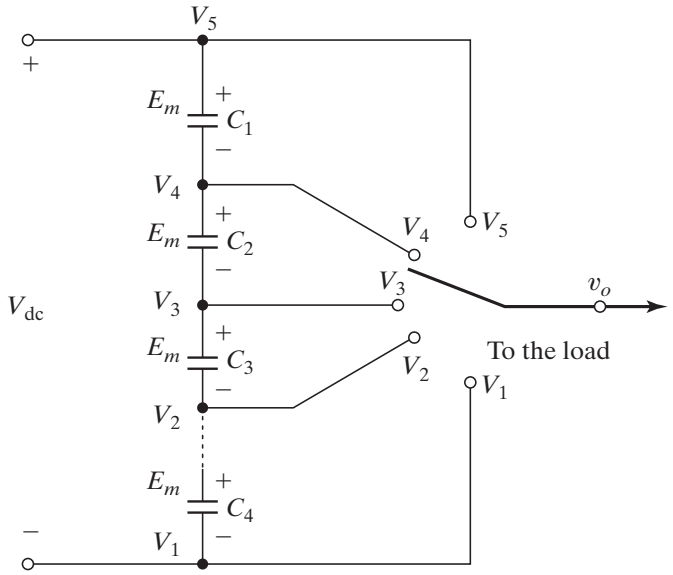
device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating. The unique structure of multilevel voltage-source inverters allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized-switching devices. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly [1, 2]. The input is a dc and the output ideally should be a sine wave. The performance parameters of multilevel converters are similar to those of PWM inverters discussed in Chapter 6.

8.2 MULTILEVEL CONCEPT

Let us consider a three-phase inverter system [4], as shown in Figure 8.1a, with a dc voltage V_{dc}. Series-connected capacitors constitute the energy tank for the inverter,



(a) Three-phase multilevel power processing system



(b) Schematic of single pole of multilevel inverter by a switch

FIGURE 8.1

General topology of multilevel inverters.

providing some nodes to which the multilevel inverter can be connected. Each capacitor has the same voltage E_m, which is given by

$$E_m = \frac{V_{\text{dc}}}{m-1} \tag{8.1}$$

where m denotes the number of levels. The term *level* is referred to as the number of nodes to which the inverter can be accessible. An m-level inverter needs $(m-1)$ capacitors.

Output phase voltages can be defined as voltages across output terminals of the inverter and the ground point denoted by o in Figure 8.1a. Moreover, input node voltages and currents can be referred to input terminal voltages of the inverter with reference to ground point and the corresponding currents from each node of the capacitors to the inverter, respectively. For example, input node (dc) voltages are designated by V_1, V_2, etc., and the input node (dc) currents by I_1, I_2, etc., as shown in Figure 8.1a. V_a, V_b, and V_c are the root-mean-square (rms) values of the line load voltages; I_a, I_b, and I_c are the rms values of the line load currents. Figure 8.1b shows the schematic of a pole in a multilevel inverter where v_o indicates an output phase voltage that can assume any voltage level depending on the selection of node (dc) voltage V_1, V_2, etc. Thus, a pole in a multilevel inverter can be regarded as a single-pole, multiple-throw switch. By connecting the switch to one node at a time, one can obtain the desired output. Figure 8.2 shows the typical output voltage of a five-level inverter.

The actual realization of the switch requires bidirectional switching devices for each node. The topological structure of multilevel inverter must (1) have less switching devices as far as possible, (2) be capable of withstanding very high input voltage for high-power applications, and (3) have lower switching frequency for each switching device.

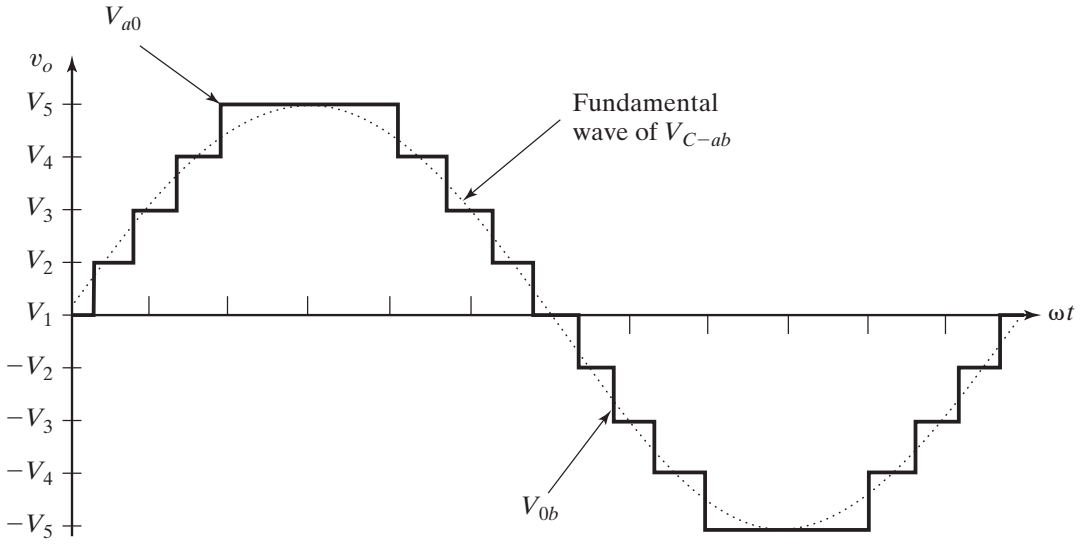


FIGURE 8.2

Typical output voltage of a five-level multilevel inverter.

8.3 TYPES OF MULTILEVEL INVERTERS

The general structure of the multilevel converter is to synthesize a near sinusoidal voltage from several levels of dc voltages, typically obtained from capacitor voltage sources. As the number of levels increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases. As the number of levels increases, the voltage that can be spanned by summing multiple voltage levels also increases. The output voltage during the positive half-cycle can be found from

$$v_{ao} = \sum_{n=1}^{m} E_n SF_n \tag{8.2}$$

where SF_n is the switching or control function of nth node and it takes a value of 0 or 1. Generally, the capacitor terminal voltages E_1, E_2, . . . all have the same value E_m. Thus, the peak output voltage is $v_{ao(\text{peak})} = (m-1)E_m = V_{\text{dc}}$. To generate an output voltage with both positive and negative values, the circuit topology has another switch to produce the negative part v_{ob} so that $v_{ab} = v_{ao} + v_{ob} = v_{ao} - v_{bo}$.

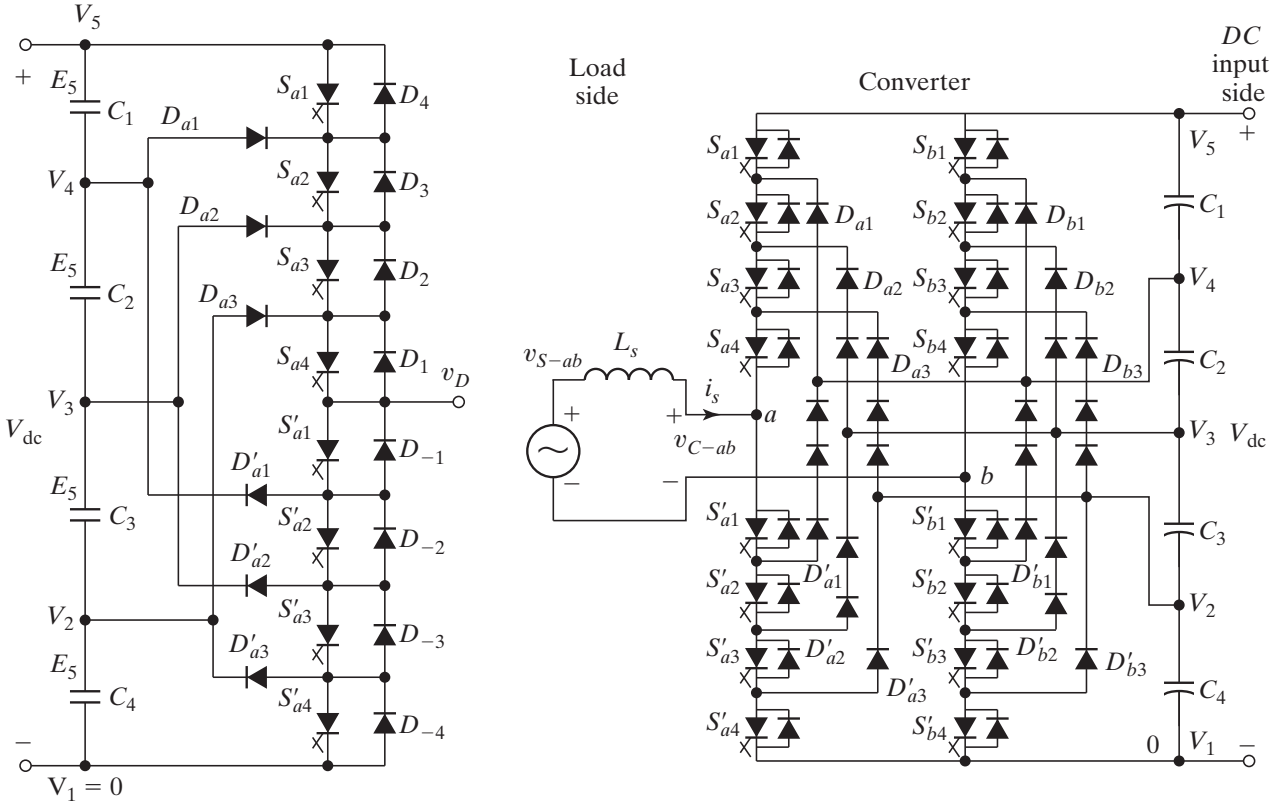
The multilevel inverters can be classified into three types [5].

Diode-clamped multilevel inverter;
Flying-capacitors multilevel inverter;
Cascade multilevel inverter.

There are three types of diode-clamped multilevel inverters—basic, improved, and modified. The modified version has many advantages. The flying-capacitor type uses capacitors instead of clamping diodes and their performances are similar to those of diode-clamped inverters. The cascade-type consists of half-bridge inverters, and the quality of the output waveforms is superior to those of other types. However, each half-bridge requires a separate dc supply. Unlike the diode-clamp or flying-capacitors inverters, the cascaded inverter does not require any voltage-clamping diodes or voltage-balancing capacitors.

8.4 DIODE-CLAMPED MULTILEVEL INVERTER

A diode-clamped multilevel (m-level) inverter (DCMLI) typically consists of $(m-1)$ capacitors on the dc bus and produces m levels on the phase voltage. Figure 8.3a shows one leg and Figure 8.3b shows a full-bridge five-level diode-clamped converter. The numbering order of the switches is S_{a1}, S_{a2}, S_{a3}, S_{a4}, S'_{a1}, S'_{a2}, S'_{a3}, and S'_{a4}. The dc bus consists of four capacitors, C_1, C_2, C_3, and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{\text{dc}}/4$, and each device voltage stress is limited to one capacitor voltage level $V_{\text{dc}}/4$ through clamping diodes. An m-level inverter leg requires $(m-1)$ capacitors, $2(m-1)$ switching devices, and $(m-1)(m-2)$ clamping diodes.



(a) One leg of a bridge

(b) Single-phase bridge

FIGURE 8.3

Diode-clamped five-level bridge multilevel inverter. [Ref. 4]

8.4.1 Principle of Operation

To produce a staircase-output voltage, let us consider only one leg of the five-level inverter, as shown in Figure 8.3a, as an example. A single-phase bridge with two legs is shown in Figure 8.3b. The *dc rail* 0 is the reference point of the output phase voltage. The steps to synthesize the five-level voltages are as follows:

1. For an output voltage level $v_{ao} = V_{dc}$, turn on all upper-half switches S_{a1} through S_{a4}.
2. For an output voltage level $v_{ao} = 3V_{dc}/4$, turn on three upper switches S_{a2} through S_{a4} and one lower switch S'_{a1}.
3. For an output voltage level $v_{ao} = V_{dc}/2$, turn on two upper switches S_{a3} through S_{a4} and two lower switches S'_{a1} and S'_{a2}.
4. For an output voltage level $v_{ao} = V_{dc}/4$, turn on one upper switch S_{a4} and three lower switches S'_{a1} through S'_{a3}.
5. For an output voltage level $v_{ao} = 0$, turn on all lower half switches S'_{a1} through S'_{a4}.

Table 8.1 shows the voltage levels and their corresponding switch states. State condition 1 means the switch is on, and state 0 means the switch is off. It should be

TABLE 8.1 Diode-Clamped Voltage Levels and Their Switch States

	Switch State							
Output v_{a0}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S'_{a1}	S'_{a2}	S'_{a3}	S'_{a4}
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

noticed that each switch is turned on only once per cycle and there are four complementary switch pairs in each phase. These pairs for one leg of the inverter are (S_{a1}, S'_{a1}), (S_{a2}, S'_{a2}), (S_{a3}, S'_{a3}), and (S_{a4}, S'_{a4}). Thus, if one of the complementary switch pairs is turned on, the other of the same pair must be off. Four switches are always turned on at the same time.

Figure 8.4 shows the phase voltage waveform of the five-level inverter. The line voltage consists of the positive phase-leg voltage of terminal *a* and the negative phase-leg voltage of terminal *b*. Each phase-leg voltage tracks one-half of the sinusoidal wave. The resulting line voltage is a nine-level staircase wave. This implies that an *m*-level converter has an *m*-level output phase-leg voltage and a $(2m - 1)$-level output line voltage.

8.4.2 Features of Diode-Clamped Inverter

The main features are as follows:

1. *High-voltage rating for blocking diodes*: Although each switching device is only required to block a voltage level of $V_{dc}/(m - 1)$, the clamping diodes need to have different reverse voltage blocking ratings. For example, when all lower

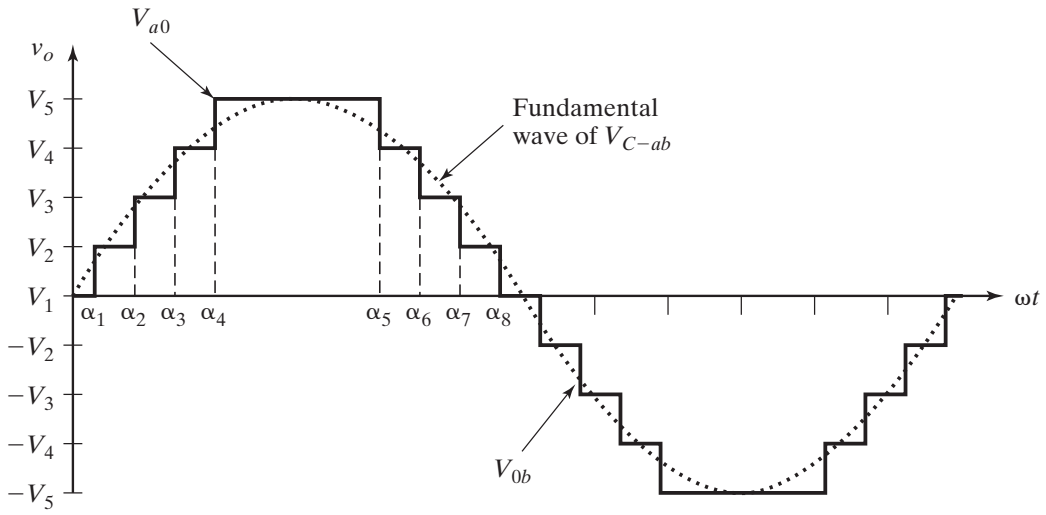


FIGURE 8.4

Phase and fundamental voltage waveforms of a five-level inverter.

devices S'_{a1} through S'_{a4} are turned on, diode D'_{a1} needs to block three capacitor voltages, or $3V_{\text{dc}}/4$. Similarly, diodes D_{a2} and D'_{a2} need to block $2V_{\text{dc}}/4$, and D_{a3} needs to block $V_{\text{dc}}/4$. Even though each main switch is supposed to block the nominal blocking voltage, the blocking voltage of each clamping diode in the diode clamping inverter is dependent on its position in the structure. In an m-level leg, there can be two diodes, each seeing a blocking voltage of

$$V_D = \frac{m - 1 - k}{m - 1} V_{\text{dc}} \tag{8.3}$$

where m is the number of levels;
k goes from 1 to $(m - 2)$;
V_{dc} is the total dc-link voltage.

If the blocking voltage rating of each diode is the same as that of the switching device, the number of diodes required for each phase is $N_D = (m - 1) \times (m - 2)$. This number represents a quadratic increase in m. Thus, for $m = 5$, $N_D = (5 - 1) \times (5 - 2) = 12$. When m is sufficiently high, the number of diodes makes the system impractical to implement, which in effect limits the number of levels.

2. *Unequal switching device rating*: We can notice from Table 8.1 that switch S_{a1} conducts only during $v_{ao} = V_{\text{dc}}$, whereas switch S_{a4} conducts over the entire cycle except during the interval when $v_{ao} = 0$. Such an unequal conduction duty requires different current ratings for the switching devices. Therefore, if the inverter design uses the average duty cycle to find the device ratings, the upper switches may be oversized, and the lower switches may be undersized. If the design uses the worst-case condition, then each phase has $2 \times (m - 2)$ upper devices oversized.
3. *Capacitor voltage unbalance*: Because the voltage levels at the capacitor terminals are different, the currents supplied by the capacitors are also different. When operating at unity power factor, the discharging time for inverter operation (or charging time for rectifier operation) for each capacitor is different. Such a capacitor charging profile repeats every half-cycle, and the result is unbalanced capacitor voltages between different levels. This voltage unbalance problem in a multilevel converter can be resolved by using approaches such as replacing capacitors by a controlled constant dc voltage source, PWM voltage regulators, or batteries.

The major advantages of the diode-clamped inverter can be summarized as follows:

- When the number of levels is high enough, the harmonic content is low enough to avoid the need for filters.
- Inverter efficiency is high because all devices are switched at the fundamental frequency.
- The control method is simple.

The major disadvantages of the diode-clamped inverter can be summarized as follows:

- Excessive clamping diodes are required when the number of levels is high.
- It is difficult to control the real power flow of the individual converter in multi-converter systems.

8.4.3 Improved Diode-Clamped Inverter

The problem of multiple blocking voltages of the clamping diodes can be addressed by connecting an appropriate number of diodes in series, as shown in Figure 8.5. However, due to mismatches of the diode characteristics, the voltage sharing is not equal. An improved version of the diode-clamped inverter [6] is shown in Figure 8.6 for five levels. The numbering order of the switches is S_1, S_2, S_3, S_4, S'_1, S'_2, S'_3, and S'_4. There are a total of 8 switches and 12 diodes of equal voltage rating, which are

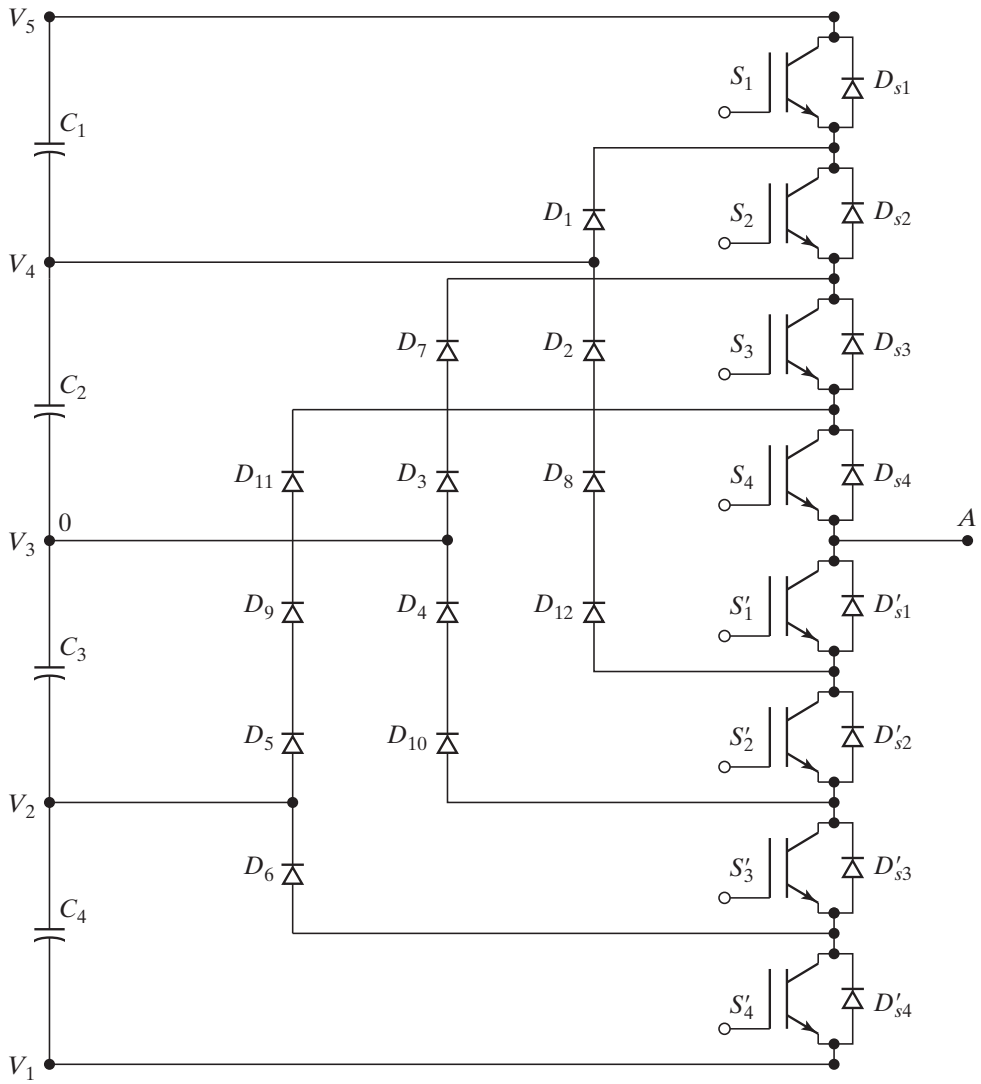


FIGURE 8.5

Diode-clamped multilevel inverter with diodes in series. [Ref. 6]

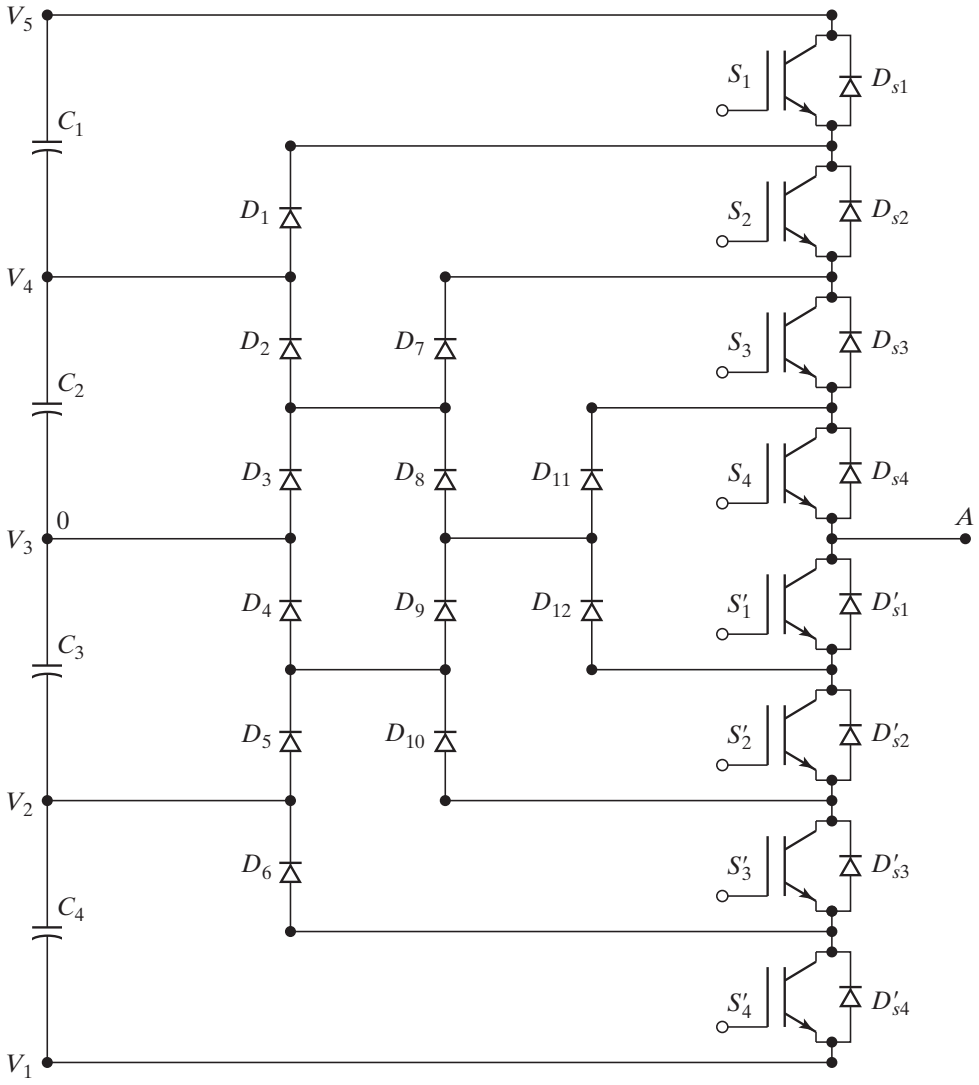


FIGURE 8.6

Modified diode-clamped inverter with distributed clamping diodes. [Ref. 6]

the same as the diode-clamping inverter with series-connected diodes. This pyramid architecture is extensible to any level, unless otherwise practically limited. A five-level inverter leg requires $(m - 1 =)$ 4 capacitors, $(2(m - 1) =)$ 8 switches, and $((m - 1)(m - 2) =)12$ clamping diodes.

Principle of operation. The modified diode-clamped inverter can be decomposed into two-level switching cells. For an m-level inverter, there are $(m - 1)$ switching cells. Thus, for $m = 5$, there are 4 cells: In cell 1, S_2, S_3, and S_4 are always on whereas S_1 and S'_1 are switched alternatively to produce an output voltage $V_{dc}/2$ and $V_{dc}/4$, respectively. Similarly, in cell 2, S_3, S_4, and S'_1 are always on whereas S_2 and S'_2 are switched alternatively to produce an output voltage $V_{dc}/4$ and 0, respectively. In cell 3, S_4, S'_1, and S'_2 are always on whereas S_3 and S'_3 are switched alternatively to produce an output voltage 0 and $-V_{dc}/2$, respectively. In final cell 4, S'_1, S'_2, and S'_3 are

always on whereas S_4 and S'_4 are switched alternatively to produce an output voltage $-V_{dc}/4$ and $-V_{dc}/2$, respectively.

Each switching cell works actually as a normal two-level inverter, except that each forward or freewheeling path in the cell involves $(m-1)$ devices instead of only one. Taking cell 2 as an example, the forward path of the up-arm involves D_1, S_2, S_2, and S_4, whereas the freewheeling path of the up-arm involves S'_1, D_{12}, D_8, and D_2, connecting the inverter output to $V_{dc}/4$ level for either positive or negative current flow. The forward path of the down-arm involves S'_1, S'_2, D_{10}, and D_4, whereas the freewheeling path of the down-arm involves D_3, D_7, S_3, and S_4, connecting the inverter output to zero level for either positive or negative current flow. The following rules govern the switching of an m-level inverter:

1. At any moment, there must be $(m-1)$ neighboring switches that are on.
2. For each two neighboring switches, the outer switch can only be turned on when the inner switch is on.
3. For each two neighboring switches, the inner switch can only be turned off when the outer switch is off.

8.5 FLYING-CAPACITORS MULTILEVEL INVERTER

Figure 8.7 shows a single-phase, full-bridge, five-level converter based on a flying-capacitors multilevel inverter (FCMLI) [5]. The numbering order of the switches is S_{a1}, S_{a2}, S_{a3}, S_{a4}, S'_{a4}, S'_{a3}, S'_{a2}, and S'_{a1}. Note that the order is numbered differently from that of the diode-clamped inverter in Figure 8.3. The numbering is immaterial so long as the switches are turned on and off in the right sequence to produce the desired output waveform. Each phase leg has an identical structure. Assuming that each capacitor has the same voltage rating, the series connection of the capacitors indicates the voltage level between the clamping points. Three inner-loop balancing capacitors (C_{a1}, C_{a2}, and C_{a3}) for phase-leg a are independent from those for phase-leg b. All phase legs share the same dc-link capacitors, C_1 through C_4.

The voltage level for the flying-capacitors converter is similar to that of the diode-clamped type of converter. That is, the phase voltage v_{ao} of an m-level converter has m levels (including the reference level), and the line voltage v_{ab} has $(2m-1)$ levels. Assuming that each capacitor has the same voltage rating as the switching device, the dc bus needs $(m-1)$ capacitors for an m-level converter. The number of capacitors required for each phase is $N_C = \sum_{j=1}^{m}(m-j)$. Thus, for $m = 5$, $N_C = 10$.

8.5.1 Principle of Operation

To produce a staircase-output voltage, let us consider the one leg of the five-level inverter shown in Figure 8.7 as an example. The dc rail 0 is the reference point of the output phase voltage. The steps to synthesize the five-level voltages are as follows:

1. For an output voltage level $v_{ao} = V_{dc}$, turn on all upper-half switches S_{a1} through S_{a4}.

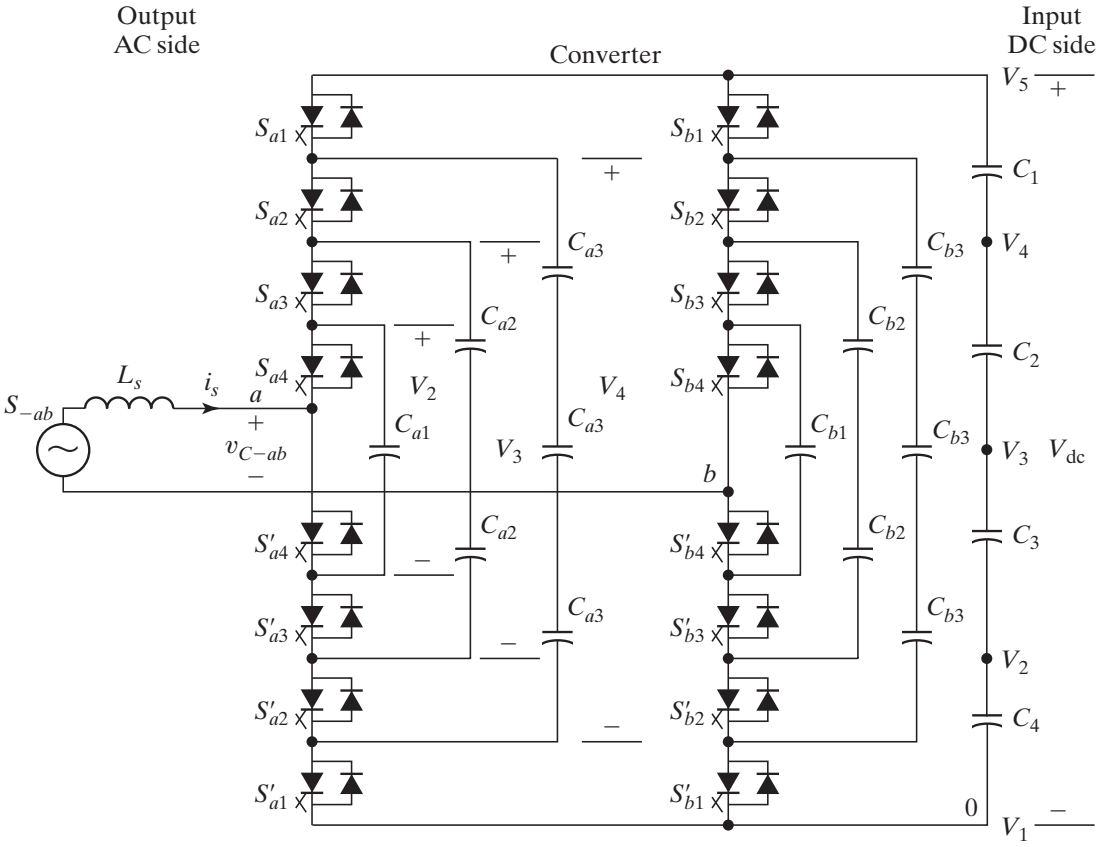


FIGURE 8.7

Circuit diagram of a five-level, flying-capacitors, single-phase inverter. [Ref. 5]

2. For an output voltage level $v_{ao} = 3V_{dc}/4$, there are four combinations:
   a. $v_{ao} = V_{dc} - V_{dc}/4$ by turning on devices S_{a1}, S_{a2}, S_{a3}, and S'_{a4}.
   b. $v_{ao} = 3V_{dc}/4$ by turning on devices S_{a2}, S_{a3}, S_{a4}, andS'_{a1}.
   c. $v_{ao} = V_{dc} - 3V_{dc}/4 + V_{dc}/2$ by turning on devices S_{a1}, S_{a3}, S_{a4}, and S'_{a2}.
   d. $v_{ao} = V_{dc} - V_{dc}/2 + V_{dc}/4$ by turning on devices S_{a1}, S_{a2}, S_{a4}, andS'_{a3}.

3. For an output voltage level $v_{ao} = V_{dc}/2$, there are six combinations:
   a. $v_{ao} = V_{dc} - V_{dc}/2$ by turning on devices S_{a1}, S_{a2}, S'_{a3}, and S'_{a4}.
   b. $v_{ao} = V_{dc}/2$ by turning on devices S_{a3}, S_{a4}, S'_{a1}, and S'_{a2}.
   c. $v_{ao} = V_{dc} - 3V_{dc}/4 + V_{dc}/2 - V_{dc}/4$ by turning on devices S_{a1}, S_{a3}, S'_{a2}, and S'_{a4}.
   d. $v_{ao} = V_{dc} - 3V_{dc}/4 + V_{dc}/4$ by turning on devices S_{a1}, S_{a4}, S'_{a2}, and S'_{a3}.
   e. $v_{ao} = 3V_{dc}/4 - V_{dc}/2 + V_{dc}/4$ by turning on devices S_{a2}, S_{a4}, S'_{a1}, and S'_{a3}.
   f. $v_{ao} = 3V_{dc}/4 - V_{dc}/4$ by turning on devices S_{a2}, S_{a3}, S'_{a1}, and S'_{a4}.

4. For an output voltage level $v_{ao} = V_{dc}/4$, there are four combinations:
   a. $v_{ao} = V_{dc} - 3V_{dc}/4$ by turning on devices S_{a1}, S'_{a2}, S'_{a3}, and S'_{a4}.
   b. $v_{ao} = V_{dc}/4$ by turning on devices S_{a4}, S'_{a1}, S'_{a2}, and S'_{a3}.
   c. $v_{ao} = V_{dc}/2 - V_{dc}/4$ by turning on devices S_{a3}, S'_{a1}, S'_{a2}, and S'_{a4}.
   d. $v_{ao} = 3V_{dc}/4 - V_{dc}/2$ by turning on devices S_{a2}, S'_{a1}, S'_{a3}, and S'_{a4}.

5. For an output voltage level $v_{ao} = 0$, turn on all lower half switches S'_{a1} through S'_{a4}.

TABLE 8.2 One Possible Switch Combination of the Flying-Capacitors Inverter

	Switch State							
Output v_{a0}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S'_{a4}	S'_{a3}	S'_{a2}	S'_{a1}
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3 = V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2 = V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

There are many possible switch combinations to generate the five-level output voltage. Table 8.2, however, lists a possible combination of the voltage levels and their corresponding switch states. Using such a switch combination requires each device to be switched only once per cycle. It can be noticed from Table 8.2 that the switching devices have unequal turn-on time. Like the diode-clamped inverter, the line voltage consists of the positive phase-leg voltage of terminal *a* and the negative phase-leg voltage of terminal *b*. The resulting line voltage is a nine-level staircase wave. This implies that an *m*-level converter has an *m*-level output phase-leg voltage and a $(2m - 1)$-level output line voltage.

8.5.2 Features of Flying-Capacitors Inverter

The main features are as follows:

1. *Large number of capacitors:* The inverter requires a large number of storage capacitors. Assuming that the voltage rating of each capacitor is the same as that of a switching device, an *m*-level converter requires a total of $(m - 1) \times (m - 2)/2$ auxiliary capacitors per phase leg in addition to $(m - 1)$ main dc bus capacitors. On the contrary, an *m*-level diode-clamp inverter only requires $(m - 1)$ capacitors of the same voltage rating. Thus, for $m = 5, N_C = 4 \times 3/2 + 4 = 10$ compared with $N_C = 4$ for the diode-clamped type.
2. *Balancing capacitor voltages:* Unlike the diode-clamped inverter, the FCMLI has redundancy at its inner voltage levels. A voltage level is redundant if two or more valid switch combinations can synthesize it. The availability of voltage redundancies allows controlling the individual capacitor voltages. In producing the same output voltage, the inverter can involve different combinations of capacitors, allowing preferential charging or discharging of individual capacitors. This flexibility makes it easier to manipulate the capacitor voltages and keep them at their proper values. It is possible to employ two or more switch combinations for middle voltage levels (i.e., $3V_{dc}/4$, $V_{dc}/2$, and $V_{dc}/4$) in one or several output cycles to balance the charging and discharging of the capacitors. Thus, by proper selection of switch combinations, the flying-capacitors multilevel converter may be used in real power conversions. However, when it involves real power conversions, the selection of a switch combination becomes very complicated, and the switching frequency needs to be higher than the fundamental frequency.

The major advantages of the flying-capacitors inverter can be summarized as follows:

- Large amounts of storage capacitors can provide capabilities during power outages.
- These inverters provide switch combination redundancy for balancing different voltage levels.
- Like the diode-clamp inverter with more levels, the harmonic content is low enough to avoid the need for filters.
- Both real and reactive power flow can be controlled.

The major disadvantages of the flying-capacitors inverter can be summarized as follows:

- An excessive number of storage capacitors is required when the number of levels is high. High-level inverters are more difficult to package with the bulky power capacitors and are more expensive too.
- The inverter control can be very complicated, and the switching frequency and switching losses are high for real power transmission.

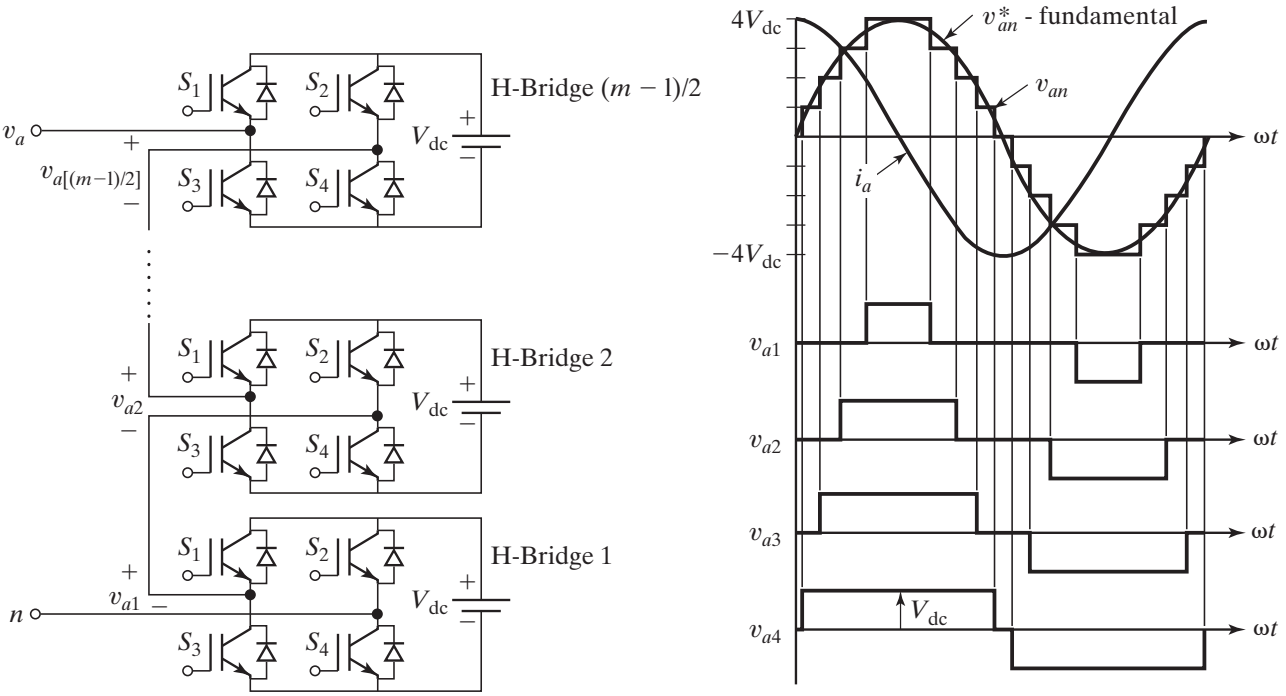
8.6 CASCADED MULTILEVEL INVERTER

A cascaded multilevel inverter consists of a series of H-bridge (single-phase, full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCSs), which may be obtained from batteries, fuel cells, or solar cells. Figure 8.8a shows the basic structure of a single-phase cascaded inverter with SDCSs [7]. Each SDCS is connected to an H-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Unlike the diode-clamp or flying-capacitors inverter, the cascaded inverter does not require any voltage-clamping diodes or voltage-balancing capacitors.

8.6.1 Principle of Operation

Figure 8.8b shows the synthesized phase voltage waveform of a five-level cascaded inverter with four SDCSs. The phase output voltage is synthesized by the sum of four inverter outputs, $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4}$. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$, by connecting the dc source to the ac output side by different combinations of the four switches, S_1, S_2, S_3, and S_4. Using the top level as the example, turning on S_1 and S_4 yields $v_{a4} = +V_{dc}$. Turning on S_2 and S_3 yields $v_{a4} = -V_{dc}$. Turning off all switches yields $v_4 = 0$. Similarly, the ac output voltage at each level can be obtained in the same manner. If N_S is the number of dc sources, the output phase voltage level is $m = N_S + 1$. Thus, a five-level cascaded inverter needs four SDCSs and four full bridges. Controlling the conducting angles at different inverter levels can minimize the harmonic distortion of the output voltage.

The output voltage of the inverter is almost sinusoidal, and it has less than 5% total harmonic distribution (THD) with each of the H-bridges switching only at fundamental frequency. If the phase current i_a, as shown in Figure 8.8b, is sinusoidal and



(a) Circuit diagram

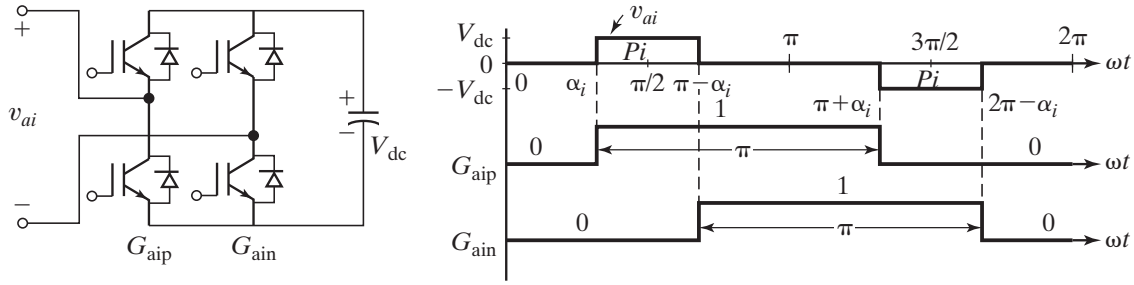
(b) Output waveform of nine-level phase voltage

FIGURE 8.8

Single-phase multilevel cascaded H-bridge inverter. [Ref. 7]

leads or lags the phase voltage v_{an} by 90°, the average charge to each dc capacitor is equal to zero over one cycle. Therefore, all SDCS capacitor voltages can be balanced.

Each H-bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase-leg-switching timings. Figure 8.9b shows the switching timings to generate a quasi-square waveform of an H-bridge in Figure 8.9a. It should be noted that each switching device always conducts for 180° (or half-cycle), regardless of the pulse width of the quasi-square wave. This switching method makes all of the switching device current stresses equal.



G_{aip}, G_{ain} is 1 if an upper switch is on and 0 if a lower switch is on

(a) One H-bridge

(b) Switching time

FIGURE 8.9

Generation of quasi-square waveform. [Ref. 7]

8.6.2 Features of Cascaded Inverter

The main features are as follows:

- For real power conversions from ac to dc and then dc to ac, the cascaded inverters need separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, and biomass.
- Connecting dc sources between two converters in a back-to-back fashion is not possible because a short circuit can be introduced when two back-to-back converters are not switching synchronously.

The major advantages of the cascaded inverter can be summarized as follows:

- Compared with the diode-clamped and flying-capacitors inverters, it requires the least number of components to achieve the same number of voltage levels.
- Optimized circuit layout and packaging are possible because each level has the same structure and there are no extra clamping diodes or voltage-balancing capacitors.
- Soft-switching techniques can be used to reduce switching losses and device stresses.

The major disadvantage of the cascaded inverter is as follows:

- It needs separate dc sources for real power conversions, thereby limiting its applications.

Example 8.1 Finding Switching Angles to Eliminate Specific Harmonics

The phase voltage waveform for a cascaded inverter is shown in Figure 8.10 for $m = 6$ (including 0 level). (a) Find the generalized Fourier series of the phase voltage. (b) Find the switching angles to eliminate the 5th, 7th, 11th, and 13th harmonics if the peak fundamental phase voltage is 80% of its maximum value. (c) Find the fundamental component B_1, THD, and the distortion factor (DF).

Solution

a. For a cascaded inverter with m levels (including 0) per half-phase, the output voltage per leg is

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + \cdots + v_{am-1} \tag{8.4}$$

Due to the quarter-wave symmetry along the x-axis, both Fourier coefficients A_0 and A_n are zero. We get B_n as

$$B_n = \frac{4V_{\text{dc}}}{\pi}\left[\int_{\alpha_1}^{\pi/2} \sin(n\omega t)\, d(\omega t) + \int_{\alpha_2}^{\pi/2} \sin(n\omega t)\, d(\omega t) + \cdots + \int_{\alpha_m-1}^{\pi/2} \sin(n\omega t)\, d(\omega t)\right] \tag{8.5}$$

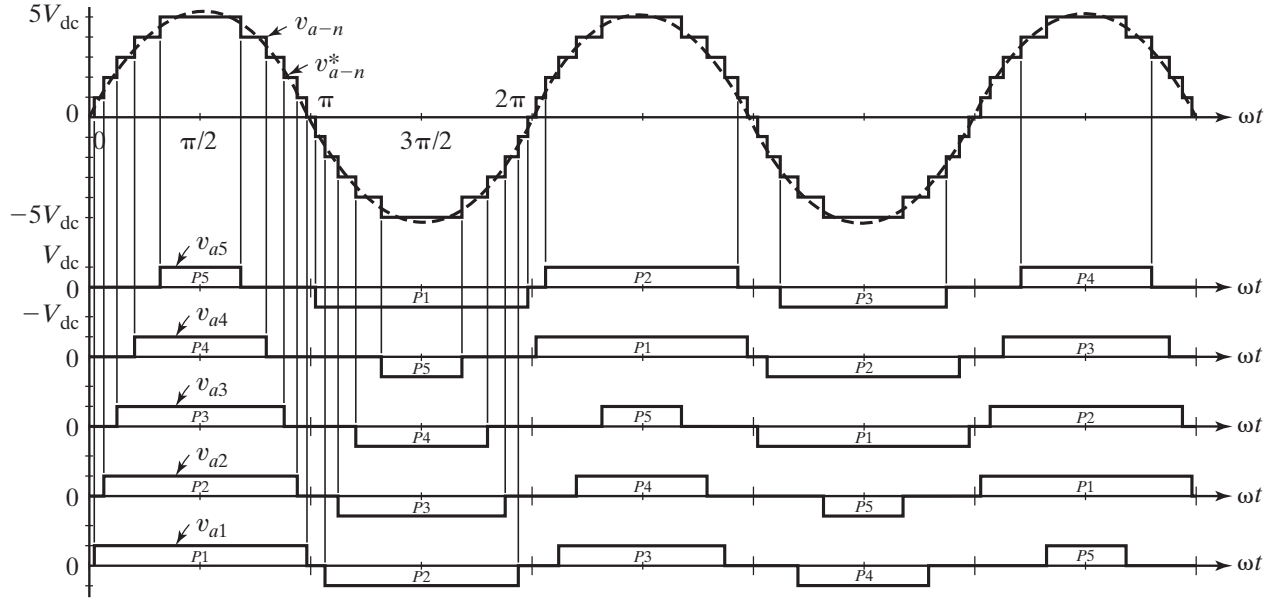


FIGURE 8.10

Switching pattern swapping of the cascade inverter for balancing battery charge. [Ref. 7]

$$B_n = \frac{4V_{\text{dc}}}{n\pi}\left[\sum_{j=1}^{m-1}\cos\left(n\alpha_j\right)\right] \tag{8.6}$$

which gives the instantaneous phase voltage v_{an} as

$$v_{an}(\omega t) = \frac{4V_{\text{dc}}}{n\pi}\left[\sum_{j=1}^{m-1}\cos\left(n\alpha_j\right)\right]\sin\left(n\omega t\right) \tag{8.7}$$

b. If the peak output phase voltage $V_{an(\text{peak})}$ must equal the carrier phase voltage, $V_{cr(\text{peak})} = (m-1)V_{\text{dc}}$. Thus, the modulation index becomes

$$M = \frac{V_{cr(\text{peak})}}{V_{an(\text{peak})}} = \frac{V_{cr(\text{peak})}}{(m-1)V_{\text{dc}}} \tag{8.8}$$

The conducting angles $\alpha_1, \alpha_2, \ldots, \alpha_{m-1}$ can be chosen such that the total harmonic distortion of the phase voltage is minimized. These angles are normally chosen so as to cancel some predominant lower frequency harmonics. Thus, to eliminate the 5th, 7th, 11th, and 13th harmonics provided that the peak fundamental phase voltage is 80% of its maximum value, we must solve the following equations for modulation index $M = 0.8$.

$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) = 0$$
$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) + \cos(7\alpha_5) = 0$$
$$\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) + \cos(11\alpha_5) = 0$$

$$\cos(13\alpha_1) + \cos(13\alpha_2) + \cos(13\alpha_3) + \cos(13\alpha_4) + \cos(13\alpha_5) = 0 \tag{8.9}$$

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) = (m-1)M = 5 \times 0.8 = 4$$

This set of nonlinear transcendental equations can be solved by an iterative method such as the Newton–Raphson method. Using Mathcad, we get

$$\alpha_1 = 6.57°, \alpha_2 = 18.94°, \alpha_3 = 27.18°, \alpha_4 = 45.15°, \text{ and } \alpha_5 = 62.24°$$

Thus, if the inverter output is symmetrically switched during the positive half-cycle of the fundamental voltage to $+V_{dc}$ at 6.57°, $+2V_{dc}$ at 18.94°, $+3V_{dc}$ at 27.18°, $+4V_{dc}$ at 45.15°, and $+5V_{dc}$ at 62.24° and similarly in the negative half-cycle to $-V_{dc}$ at 186.57°, $-2V_{dc}$ at 198.94°, $-3V_{dc}$ at 207.18°, $-4V_{dc}$ at 225.15°, and $-5V_{dc}$ at 242.24°, the output voltage cannot contain the 5th, 7th, 11th, and 13th harmonics.

c. Using Mathcad, we get $B_1 = 5.093\%$, THD $= 5.975\%$, and DF $= 0.08\%$

Note: The duty cycle for each of the voltage levels is different. This means that the level-l dc source discharges much sooner than the level-5 dc source. However, by using a switching pattern-swapping scheme among the various levels every half-cycle, as shown in Figure 8.10, all batteries can be equally used (discharged) or charged [7]. For example, if the first pulse sequence is P_1, P_2, …, P_5, then the next sequence is P_2, P_3, P_4, P_5, P_1, and so on.

8.7 APPLICATIONS

There is considerable interest in applying voltage source inverters in high-power applications such as in utility systems for controlled sources of reactive power. In the steady-state operation, an inverter can produce a controlled reactive current and operates as a static volt–ampere reactive (VAR)-compensator (STATCON). Also, these inverters can reduce the physical size of the compensator and improve its performance during power system contingencies. The use of a high-voltage inverter makes possible direct connection to the high-voltage (e.g., 13-kV) distribution system, eliminating the distribution transformer and reducing system cost. In addition, the harmonic content of the inverter waveform can be reduced with appropriate control techniques and thus the efficiency of the system can be improved. The most common applications of multilevel converters include (1) reactive power compensation, (2) back-to-back intertie, and (3) variable speed drives.

8.7.1 Reactive Power Compensation

An inverter converts a dc voltage to an ac voltage; with a phase shift of 180°, the inverter can be operated as a dc–ac converter, that is, a controlled rectifier. With a purely capacitive load, the inverter operating as a dc–ac converter can draw reactive current from the ac supply. Figure 8.11 shows the circuit diagram of a multilevel converter directly connected to a power system for reactive power compensation. The load side is connected to the ac supply and the dc side is open, not connected to any dc voltage.

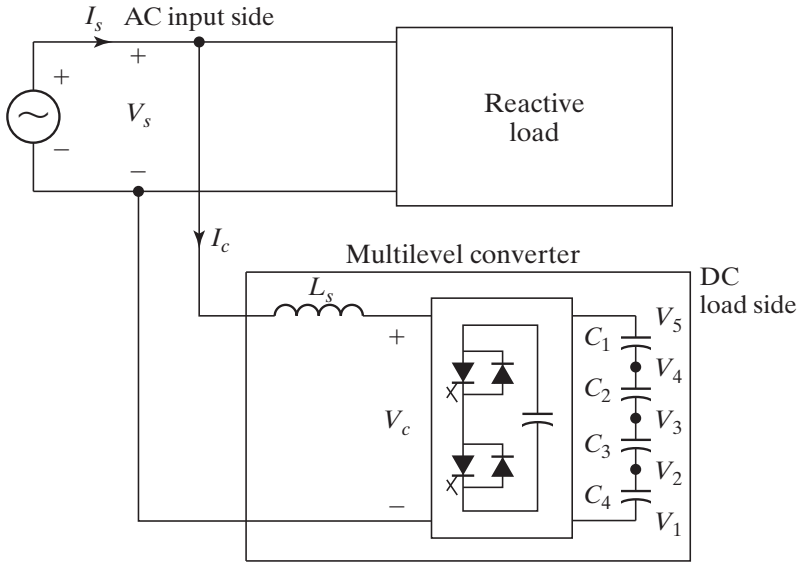


FIGURE 8.11

A multilevel converter connected to a power system for reactive power compensation. [Ref. 5]

For the control of the reactive power flow, the inverter gate control is phase shifted by 180°. The dc side capacitors act as the load.

When a multilevel converter draws pure reactive power, the phase voltage and current are 90° apart, and the capacitor charge and discharge can be balanced. Such a converter, when serving for reactive power compensation, is called a static-VAR generator (SVG). All three multilevel converters can be used in reactive power compensation without having the voltage unbalance problem.

The relationship of the source voltage vector $\mathbf{V_S}$ and the converter voltage vector $\mathbf{V}_C$ is simply $\mathbf{V}_S = \mathbf{V}_C + j\mathbf{I_C}X_S$, where $\mathbf{I_C}$ is the converter current vector, and X_S is the reactance of the inductor L_S. Figure 8.12a illustrates that the converter voltage is in phase with the source voltage with a leading reactive current, whereas Figure 8.12b illustrates a lagging reactive current. The polarity and the magnitude of the reactive current are controlled by the magnitude of the converter voltage $\mathbf{V_C}$, which is a function of the dc bus voltage and the voltage modulation index, as expressed by Eqs. (8.7) and (8.8).

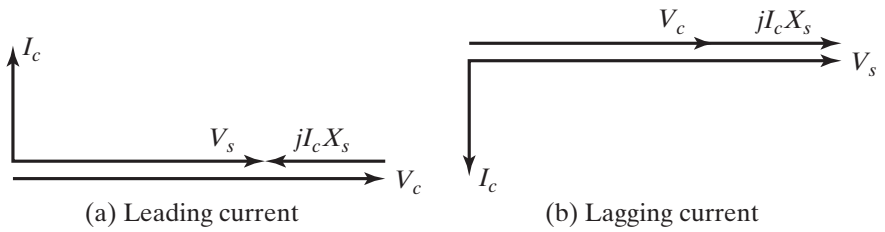


FIGURE 8.12

Phasor diagrams of the source and the converter voltages for reactive power compensation.

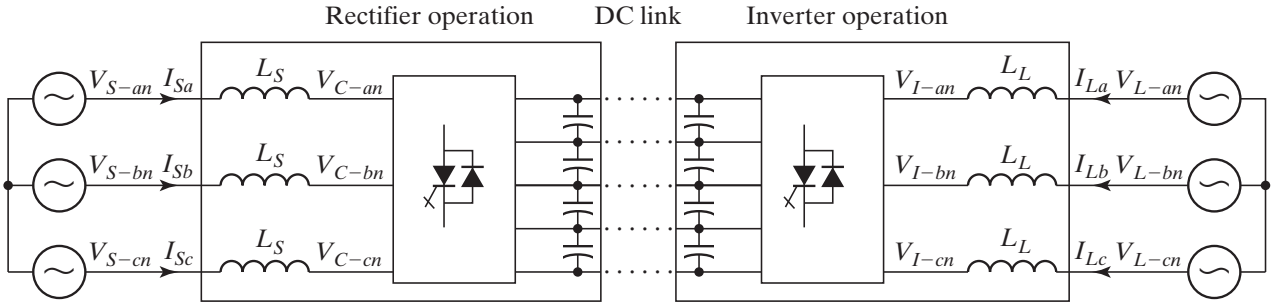


FIGURE 8.13

Back-to-back intertie system using two diode-clamped multilevel converters. [Ref. 5]

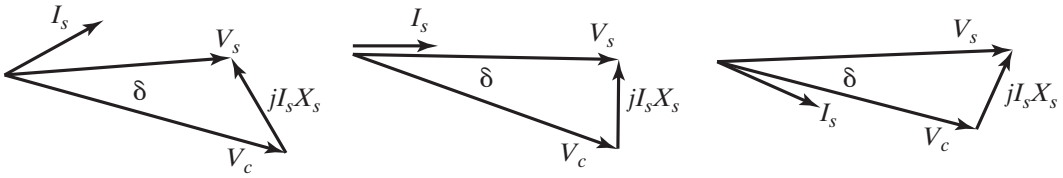
8.7.2 Back-to-Back Intertie

Figure 8.13 shows two diode-clamped multilevel converters that are interconnected with a dc capacitor link. The left-hand side converter serves as the rectifier for utility interface, and the right-hand side converter serves as the inverter to supply the ac load. Each switch remains on once per fundamental cycle. The voltage across each capacitor remains well balanced, while maintaining the staircase voltage wave, because the unbalance capacitor voltages on both sides tend to compensate each other. Such a dc capacitor link is categorized as the back-to-back intertie.

The back-to-back intertie that connects two asynchronous systems can be regarded as (1) a frequency changer, (2) a phase shifter, or (3) a power flow controller. The power flow between two systems can be controlled bidirectionally. Figure 8.14 shows the phasor diagram for real power transmission from the source end to the load end. This diagram indicates that the source current can be leading or in-phase or lagging the source voltage. The converter voltage is phase shifted from the source voltage with a power angle, δ. If the source voltage is constant, then the current or power flow can be controlled by the converter voltage. For $\delta = 0$, the current is either 90° leading or lagging, meaning that only reactive power is generated.

8.7.3 Adjustable Speed Drives

The back-to-back intertie can be applied to a utility compatible adjustable speed drive (ASD) where the input is the constant frequency ac source from the utility supply and the output is the variable frequency ac load. For an ideal utility compatible system, it requires unity power factor, negligible harmonics, no electromagnetic interference



(a) Leading power factor (b) Unity power factor (c) Lagging power factor

FIGURE 8.14

Phasor diagram of the source voltage, converter voltage, and current showing real power conversions.

(EMI), and high efficiency. The major differences, when using the same structure for ASDs and for back-to-back interties, are the control design and the size of the capacitor. Because the ASD needs to operate at different frequencies, the dc-link capacitor needs to be well sized to avoid a large voltage swing under dynamic conditions.

8.8 SWITCHING DEVICE CURRENTS

Let us take a three-level half-bridge inverter, as shown in Figure 8.15a, where V_o and I_0 indicate the rms load voltage and current, respectively. Assuming that the load inductance is sufficiently large and the capacitors maintain their voltages so that the output current is sinusoidal as given by

$$i_o = I_m \sin(\omega t - \phi) \tag{8.10}$$

where I_m is the peak value of the load current, and ϕ is the load impedance angle.

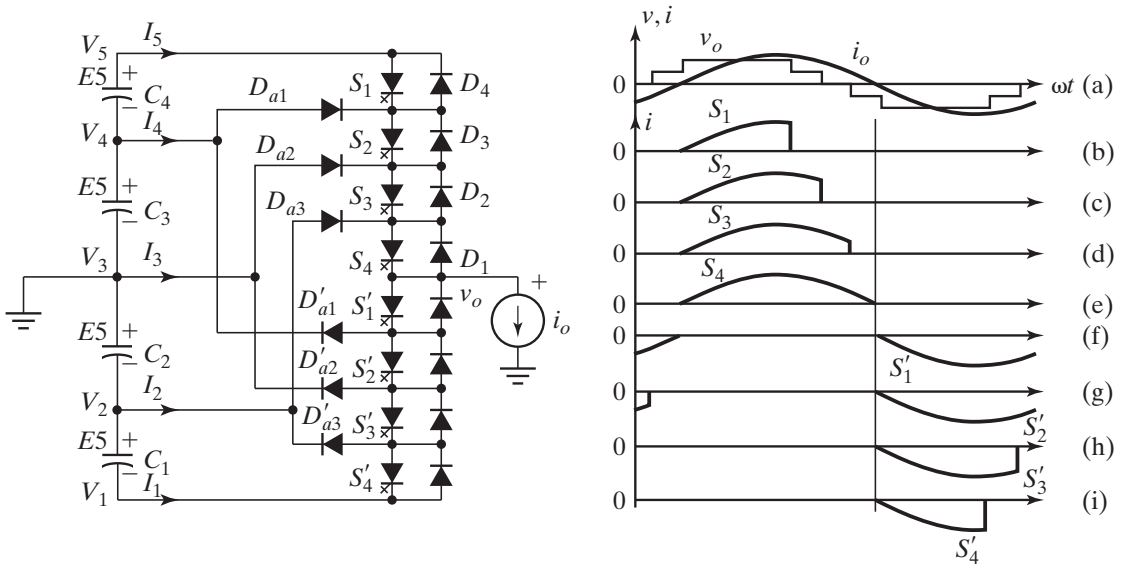
Figure 8.15b shows a typical current waveform of each switching device with a simple stepped control of output phase voltage. The most inner switches such as S_4 and S_1' carry more current than the most outer switches such as S_1 and S_4'.

Each input node current can be expressed as a function of the switching function SF_n as given by

$$i_n = SF_n i_o \quad \text{for } n = 1,2,\ldots,m \tag{8.11}$$

Because the single-pole multiple-throw switch multilevel inverter, shown in Figure 8.1b, is always connected to one and only one input node at every instant, the output load current could be drawn from one and only one input node. That is,

$$i_o = \sum_{n=1}^{m} i_n \tag{8.12}$$



(a) Five-level inverter circuit (b) Current waveforms

FIGURE 8.15

Half-bridge three-level diode-clamped inverter. [Ref. 4]

and the rms value of each current is expressed as

$$I_o^2(\text{rms}) = \sum_n^m I_n^2(\text{rms}) \tag{8.13}$$

where $I_{n(\text{rms})}$ is the rms current of the nth node given by

$$I_{n(\text{rms})} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} SF_n i_o^2\, d(\omega t)} \quad \text{for } n = 1, 2, \ldots, m \tag{8.14}$$

For balanced switching with respect to the ground level, we get

$$i_{1(\text{rms})}^2 = i_{5(\text{rms})}^2, \text{ and } i_{2(\text{rms})}^2 = i_{4(\text{rms})}^2 \tag{8.15}$$

It should be noted that by structure, the currents through the opposite switches such as $S_1', \ldots, S_4'$ would have the same rms current through $S_4, \ldots, S_1$, respectively.

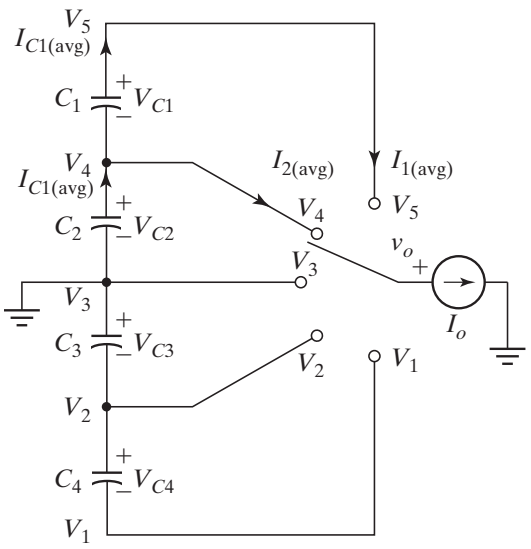
8.9 DC-LINK CAPACITOR VOLTAGE BALANCING

The voltage balancing of capacitors acting as an energy tank is very important for the multilevel inverter to work satisfactorily. Figure 8.16a shows the schematic of a half-bridge inverter with five levels and Figure 8.16b illustrates the stepped-output voltage and the sinusoidal load current $i_o = I_m \sin(\omega t - \phi)$.

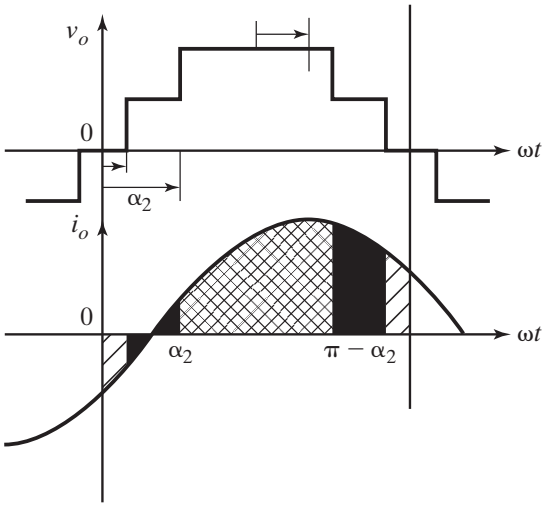
The average value of the input node current i_1 is given by

$$I_{1(\text{avg})} = \frac{1}{2\pi}\int_{\alpha_2}^{\pi-\alpha_2} i_o\, d(\omega t) = \frac{1}{2\pi}\int_{\alpha_2}^{\pi-\alpha_2} I_m \sin(\omega t - \phi)\, d(\omega t)$$

$$= \frac{I_m}{\pi}\cos\phi\cos\alpha_2 \tag{8.16}$$



(a) Schematic of a three-level half-bridge inverter



(b) Distribution of load current

FIGURE 8.16

Charge distribution of capacitors. [Ref. 4]

Similarly, the average value of the input node current i_2 is given by

$$I_{2(\text{avg})} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2} i_o d(\omega t) = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2} I_m \sin(\omega t - \phi)\, d(\omega t)$$

$$= \frac{I_m}{\pi}\cos\phi(\cos\alpha_1 - \cos\alpha_2) \tag{8.17}$$

By symmetry, $I_{3(\text{avg})} = 0$, $I_{4(\text{avg})} = -I_{2(\text{avg})}$, and $I_{5(\text{avg})} = -I_{1(\text{avg})}$. Thus, each capacitor voltage should be regulated so that each capacitor supplies the average current per cycle as follows:

$$I_{C1(\text{avg})} = I_{1(\text{avg})} = \frac{I_m}{\pi}\cos\phi\cos\alpha_2 \tag{8.18}$$

$$I_{C2(\text{avg})} = I_{1(\text{avg})} + I_{2(\text{avg})} = \frac{I_m}{\pi}\cos\phi\cos\alpha_1 \tag{8.19}$$

Therefore, $I_{C1(\text{avg})} < I_{C2(\text{avg})}$ for $\alpha_1 < \alpha_2$. This results in the capacitor charge unbalancing, and more charge flows from the inner capacitor C_2 (or C_3) than that of the outer capacitor C_1 (or C_4). Thus, each capacitor voltage should be regulated to supply the appropriate amount of average current; otherwise, its voltage V_{C2} (or V_{C3}) goes to the ground level as time goes. Equations (8.18) and (8.19) can be extended to the nth capacitor of a multilevel converter as given by

$$I_{Cn(\text{avg})} = \frac{I_m}{\pi}\cos\phi\cos\alpha_n \tag{8.20}$$

Equations (8.18) and (8.19) give

$$\frac{\cos\alpha_2}{\cos\alpha_1} = \frac{I_{C2(\text{avg})}}{I_{C1(\text{avg})}} \tag{8.21}$$

which can be generalized for the nth and $(n-1)$th capacitors

$$\frac{\cos\alpha_n}{\cos\alpha_{n-1}} = \frac{I_{Cn(\text{avg})}}{I_{C(n-1)(\text{avg})}} \tag{8.22}$$

which means that the capacitor charge unbalancing exists regardless of the load condition and it depends on the control strategy such as $\alpha_1, \alpha_2, \ldots, \alpha_n$. Applying control strategy that forces the energy transfer from the outer capacitors to the inner capacitors can solve this unbalancing problem [8–11].

8.10 FEATURES OF MULTILEVEL INVERTERS

A multilevel inverter can eliminate the need for the step-up transformer and reduce the harmonics produced by the inverter. Although the multilevel inverter structure was initially introduced as a means of reducing the output waveform harmonic content, it was found [1] that the dc bus voltage could be increased beyond the voltage rating

of an individual power device by the use of a voltage-clamping network consisting of diodes. A multilevel structure with more than three levels can significantly reduce the harmonic content [2, 3]. By using voltage-clamping techniques, the system KV rating can be extended beyond the limits of an individual device. The intriguing feature of the multilevel inverter structures is their ability to scale up the kilovolt–ampere (KVA)-rating and also to improve the harmonic performance greatly without having to resort to PWM techniques. The key features of a multilevel structure follow:

- The output voltage and power increase with number of levels. Adding a voltage level involves adding a main switching device to each phase.
- The harmonic content decreases as the number of levels increases and filtering requirements are reduced.
- With additional voltage levels, the voltage waveform has more free-switching angles, which can be preselected for harmonic elimination.
- In the absence of any PWM techniques, the switching losses can be avoided. Increasing output voltage and power does not require an increase in rating of individual device.
- Static and dynamic voltage sharing among the switching devices is built into the structure through either clamping diodes or capacitors.
- The switching devices do not encounter any voltage-sharing problems. For this reason, multilevel inverters can easily be applied for high-power applications such as large motor drives and utility supplies.
- The fundamental output voltage of the inverter is set by the dc bus voltage V_{dc}, which can be controlled through a variable dc link.

8.11 COMPARISONS OF MULTILEVEL CONVERTERS

The multilevel converters [8] can replace the existing systems that use traditional multipulse converters without the need for transformers. For a three-phase system, the relationship between the number of levels m, and the number of pulses p, can be formulated by $p = 6 \times (m - 1)$. All three converters have the potential for applications in high-voltage, high-power systems such as an SVG without voltage unbalance problems because the SVG does not draw real power. The diode-clamped converter is most suitable for the back-to-back intertie system operating as a unified power flow controller. The other two types may also be suitable for the back-to-back intertie, but they would require more switching per cycle and more advanced control techniques to balance the voltage. The multilevel inverters can find potential applications in adjustable speed drives where the use of multilevel converters can not only solve harmonics and EMI problems but also avoid possible high-frequency switching dv/dt-induced motor failures.

Table 8.3 compares the component requirements per phase leg among the three multilevel converters. All devices are assumed to have the same voltage rating, but not necessarily the same current rating. The cascaded inverter uses a full bridge in each level as compared with the half-bridge version for the other two types. The cascaded inverter requires the least number of components and has the potential for utility interface applications because of its capabilities for applying modulation and soft-switching techniques.

TABLE 8.3 Comparisons of Component Requirements per Leg of Three Multilevel Converters [Ref. 5]

Converter Type	Diode Clamp	Flying Capacitors	Cascaded Inverters
Main switching devices	$(m-1)\times 2$	$(m-1)\times 2$	$(m-1)\times 2$
Main diodes	$(m-1)\times 2$	$(m-1)\times 2$	$(m-1)\times 2$
Clamping diodes	$(m-1)\times(m-2)$	0	0
Dc bus capacitors	$(m-1)$	$(m-1)$	$(m-1)/2$
Balancing capacitors	0	$(m-1)\times(m-2)/2$	0

SUMMARY

Multilevel converters can be applied to utility interface systems and motor drives. These converters offer a low output voltage THD, and a high efficiency and power factor. There are three types of multilevel converters: (1) diode clamped, (2) flying capacitors, and (3) cascaded. The main advantages of multilevel converters include the following:

- They are suitable for high-voltage and high-current applications.
- They have higher efficiency because the devices can be switched at a low frequency.
- Power factor is close to unity for multilevel inverters used as rectifiers to convert ac to dc.
- No EMI problem exists.
- No charge unbalance problem results when the converters are in either charge mode (rectification) or drive mode (inversion).

The multilevel converters require balancing the voltage across the series-connected dc-bus capacitors. Capacitors tend to overcharge or completely discharge, at which condition the multilevel converter reverts to a three-level converter unless an explicit control is devised to balance the capacitor charge. The voltage-balancing technique must be applied to the capacitor during the operations of the rectifier and the inverter. Thus, the real power flow into a capacitor must be the same as the real power flow out of the capacitor, and the net charge on the capacitor over one cycle remains the same.

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REVIEW QUESTIONS

8.1 What is a multilevel converter?
8.2 What is the basic concept of multilevel converters?
8.3 What are the features of a multilevel converter?
8.4 What are the types of multilevel converters?
8.5 What is a diode-clamped multilevel inverter?
8.6 What are the advantages of a diode-clamped multilevel inverter?
8.7 What are the disadvantages of a diode-clamped multilevel inverter?
8.8 What are the advantages of a modified diode-clamped multilevel inverter?
8.9 What is a flying-capacitors multilevel inverter?
8.10 What are the advantages of a flying-capacitors multilevel inverter?
8.11 What are the disadvantages of a flying-capacitors multilevel inverter?
8.12 What is a cascaded multilevel inverter?
8.13 What are the advantages of a cascaded multilevel inverter?
8.14 What are the disadvantages of a cascaded multilevel inverter?
8.15 What is a back-to-back intertie system?
8.16 What does the capacitor voltage unbalancing mean?
8.17 What are the possible applications of multilevel inverters?

PROBLEMS

8.1 A single-phase diode-clamped inverter has $m = 5$. Find the generalized Fourier series and THD of the phase voltage.
8.2 A single-phase diode-clamped inverter has $m = 7$. Find the peak voltage and current ratings of diodes and switching devices if $V_{dc} = 5\,\text{kV}$ and $i_o = 50\,\sin(\theta - \pi/3)$.
8.3 A single-phase diode-clamped inverter has $m = 5$. Find **(a)** instantaneous, average, and rms currents of each node, and **(b)** average and rms capacitor current if $V_{dc} = 5\,\text{kV}$ and $i_o = 50\,\sin(\theta - \pi/3)$.

8.4 A single-phase flying-capacitors multilevel inverter has $m = 5$. Find the generalized Fourier series and THD of the phase voltage.

8.5 A single-phase flying-capacitors multilevel inverter has $m = 11$. Find the number of capacitors, the peak voltage ratings of diodes and switching devices if $V_{dc} = 10\,\text{kV}$.

8.6 Compare the number of diodes and capacitors for diode clamp, flying capacitors, and cascaded inverters if $m = 9$.

8.7 A single-phase cascaded multilevel inverter has $m = 5$. Find the peak voltage, and average and rms current ratings of H-bridge if $V_{dc} = 2\,\text{kV}$ and $i_o = 200\sin(\theta - \pi/6)$.

8.8 A single-phase cascaded multilevel inverter has $m = 5$. Find the average current of each separate dc source (SDCS) if $V_{dc} = 2\,\text{kV}$ and $i_o = 300\sin(\theta - \pi/3)$.

8.9 A single-phase cascaded multilevel inverter has $m = 5$. Find the generalized Fourier series and THD of the phase voltage. **(b)** Find the switching angles to eliminate the 5th, 7th, 11th, and 13th harmonics.

8.10 A single-phase cascaded multilevel inverter has $m = 5$. **(a)** Find the generalized Fourier series and THD of the phase voltage. **(b)** Find the switching angles to eliminate the 5th, 7th, and 11th harmonics if the peak fundamental phase voltage is 60% of its maximum value.

8.11 Repeat Table 8.1 by showing the voltage levels and their corresponding switch states for a diode-clamped inverter for $m = 7$.

8.12 Repeat Table 8.1 by showing the voltage levels and their corresponding switch states for a diode-clamped inverter for $m = 9$.

8.13 Repeat Table 8.2 by showing the voltage levels and their corresponding switch states for a flying-capacitor type inverter for $m = 7$.

8.14 Repeat Table 8.2 by showing the voltage levels and their corresponding switch states for a flying-capacitor type inverter for $m = 9$.